

GSS4565

N AND P-CHANNEL ENHANCEMENT MODE POWER MOSFET

N-CH BV _{DSS}	40V
R _{DS(ON)}	25mΩ
I _D	7.6A
P-CH BV _{DSS}	-40V
R _{DS(ON)}	33mΩ
I _D	-6.5A

Description

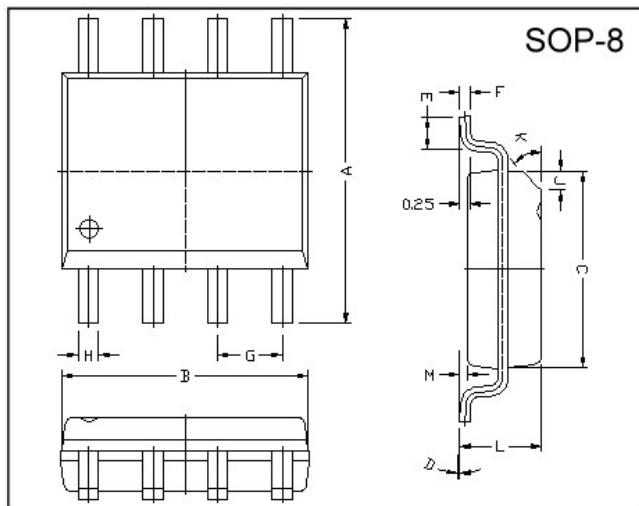
The GSS4565 provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SOP-8 package is universally preferred for all commercial-industrial surface mount applications and suited for low voltage applications such as DC/DC converters.

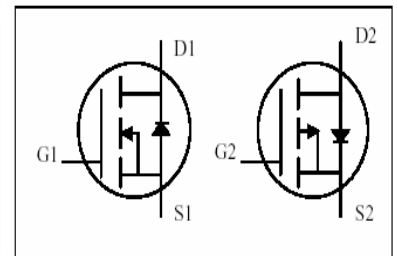
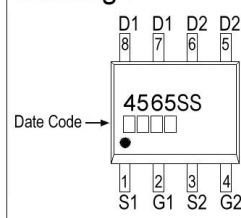
Features

- *Simple Drive Requirement
- *Lower On-resistance
- *Fast Switching Performance

Package Dimensions



Marking :



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	M	0.10	0.25
B	4.80	5.00	H	0.35	0.49
C	3.80	4.00	L	1.35	1.75
D	0°	8°	J	0.375 REF.	
E	0.40	0.90	K	45°	
F	0.19	0.25	G	1.27 TYP.	

Absolute Maximum Ratings

Parameter	Symbol	Ratings		Unit
		N-channel	P-channel	
Drain-Source Voltage	V _{DS}	40	-40	V
Gate-Source Voltage	V _{GS}	±20	±20	V
Continuous Drain Current ³	I _D @TA=25°C	7.6	-6.5	A
Continuous Drain Current ³	I _D @TA=70°C	6	-5.2	A
Pulsed Drain Current ¹	I _{DM}	30	-30	A
Total Power Dissipation	P _D @TA=25°C	2.0		W
Linear Derating Factor		0.016		W/°C
Operating Junction and Storage Temperature Range	T _j , T _{stg}	-55 ~ +150		°C

Thermal Data

Parameter	Symbol	Value	Unit
Thermal Resistance Junction-ambient ³ Max.	R _{thj-a}	62.5	°C/W

N-Channel Electrical Characteristics(T_j = 25°C Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV _{DSS}	40	-	-	V	V _{GS} =0, I _D =250uA
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_j$	-	0.03	-	V/°C	Reference to 25°C, I _D =1mA
Gate Threshold Voltage	V _{GS(th)}	1.0	-	3.0	V	V _{DS} =V _{GS} , I _D =250uA
Forward Transconductance	g _{fs}	-	12	-	S	V _{DS} =10V, I _D =7A
Gate-Source Leakage Current	I _{GSS}	-	-	±100	nA	V _{GS} = ±20V
Drain-Source Leakage Current(T _j =25°C)	I _{DSS}	-	-	1	uA	V _{DS} =40V, V _{GS} =0
Drain-Source Leakage Current(T _j =70°C)		-	-	25	uA	V _{DS} =32V, V _{GS} =0
Static Drain-Source On-Resistance ²	R _{DS(ON)}	-	-	25	mΩ	V _{GS} =10V, I _D =7A
		-	-	32		V _{GS} =4.5V, I _D =5A
Total Gate Charge ²	Q _g	-	17	27	nC	I _D =7A V _{DS} =32V V _{GS} =4.5V
Gate-Source Charge	Q _{gs}	-	4	-		
Gate-Drain ("Miller") Charge	Q _{gd}	-	10	-		
Turn-on Delay Time ²	T _{d(on)}	-	11	-	ns	V _{DS} =20V I _D =1A V _{GS} =10V R _G =3.3Ω R _D =20Ω
Rise Time	T _r	-	8	-		
Turn-off Delay Time	T _{d(off)}	-	30	-		
Fall Time	T _f	-	11	-		
Input Capacitance	C _{iss}	-	1400	2240	pF	V _{GS} =0V V _{DS} =25V f=1.0MHz
Output Capacitance	C _{oss}	-	250	-		
Reverse Transfer Capacitance	C _{rss}	-	170	-		

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward On Voltage ²	V _{SD}	-	-	1.2	V	I _S =1.7A, V _{GS} =0V, T _j =25°C
Reverse Recovery Time ²	T _{rr}	-	26	-	ns	I _S =7A, V _{GS} =0V dI/dt=100A/μs
Reverse Recovery Charge	Q _{rr}	-	21	-	nC	

Notes: 1. Pulse width limited by Max. junction temperature.

2. Pulse width ≤ 300us, duty cycle ≤ 2%.

3. Surface mounted on 1 in² copper pad of FR4 board; 135°C/W when mounted on Min. copper pad.

P-Channel Electrical Characteristics(T_j = 25°C Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Breakdown Voltage	BV _{DSS}	-40	-	-	V	V _{GS} =0, I _D =-250uA
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_j$	-	-0.03	-	V/°C	Reference to 25°C, I _D =-1mA
Gate Threshold Voltage	V _{GS(th)}	-1.0	-	-3.0	V	V _{DS} =V _{GS} , I _D =-250uA
Forward Transconductance	g _{fs}	-	10	-	S	V _{DS} =-10V, I _D =-6A
Gate-Source Leakage Current	I _{GSS}	-	-	±100	nA	V _{GS} = ±20V
Drain-Source Leakage Current(T _j =25°C)	I _{DSS}	-	-	-1	uA	V _{DS} =-40V, V _{GS} =0
Drain-Source Leakage Current(T _j =70°C)		-	-	-25	uA	V _{DS} =-32V, V _{GS} =0
Static Drain-Source On-Resistance ²	R _{DS(on)}	-	-	33	mΩ	V _{GS} =-10V, I _D =-6A
		-	-	42		V _{GS} =-4.5V, I _D =-4A
Total Gate Charge ²	Q _g	-	20	32	nC	I _D =-6A V _{DS} =-32V V _{GS} =-4.5V
Gate-Source Charge	Q _{gs}	-	4	-		
Gate-Drain ("Miller") Charge	Q _{gd}	-	10	-		
Turn-on Delay Time ²	T _{d(on)}	-	11	-	ns	V _{DS} =-20V I _D =-1A V _{GS} =-10V R _G =3.3Ω R _D =20Ω
Rise Time	T _r	-	7	-		
Turn-off Delay Time	T _{d(off)}	-	67	-		
Fall Time	T _f	-	43	-		
Input Capacitance	C _{iss}	-	1440	2300	pF	V _{GS} =0V V _{DS} =-25V f=1.0MHz
Output Capacitance	C _{oss}	-	250	-		
Reverse Transfer Capacitance	C _{rss}	-	190	-		

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Forward On Voltage ²	V _{SD}	-	-	-1.2	V	I _S =-1.7A, V _{GS} =0V, T _j =25°C
Reverse Recovery Time ²	T _{rr}	-	27	-	ns	I _S =-6A, V _{GS} =0V dI/dt=100A/μs
Reverse Recovery Charge	Q _{rr}	-	23	-	nC	

Notes: 1. Pulse width limited by Max. junction temperature.

2. Pulse width ≤ 300us, duty cycle ≤ 2%.

3. Surface mounted on 1 in² copper pad of FR4 board; 135°C/W when mounted on Min. copper pad.

Characteristics Curve N-Channel

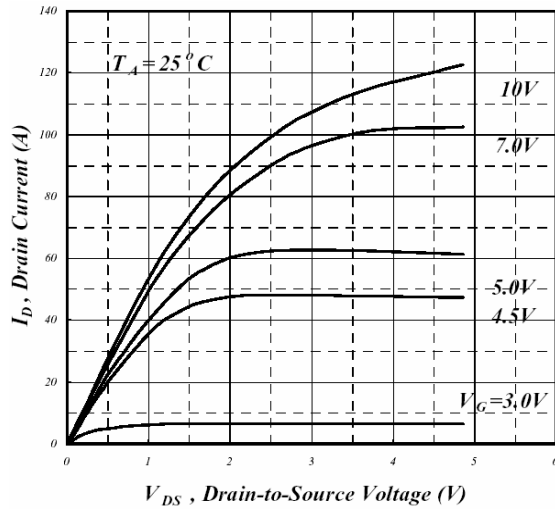


Fig 1. Typical Output Characteristics

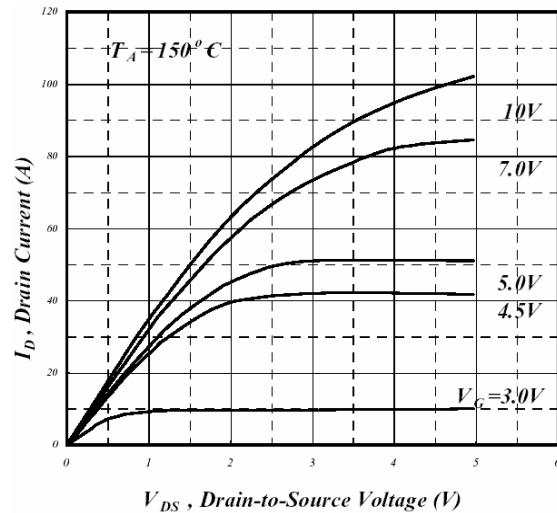


Fig 2. Typical Output Characteristics

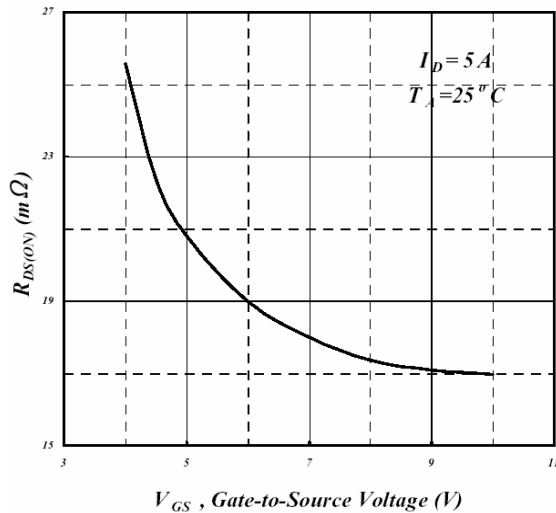


Fig 3. On-Resistance v.s. Gate Voltage

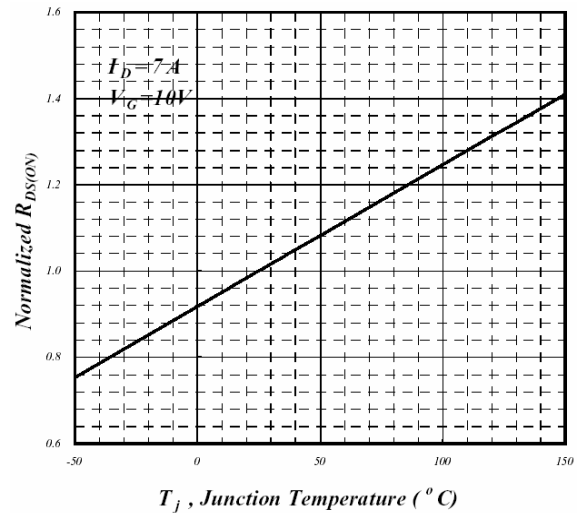


Fig 4. Normalized On-Resistance v.s. Junction Temperature

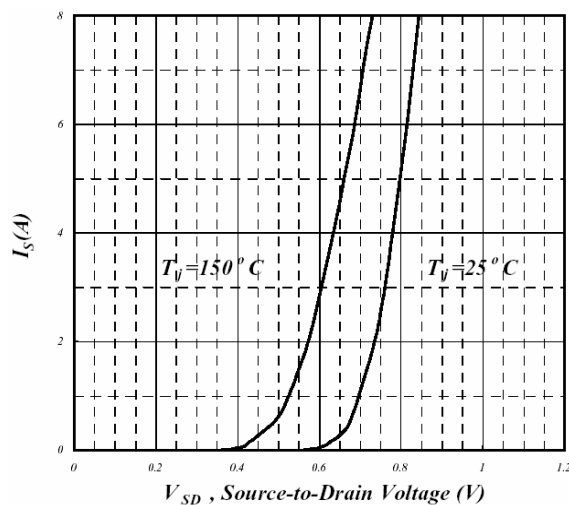


Fig 5. Forward Characteristics of Reverse Diode

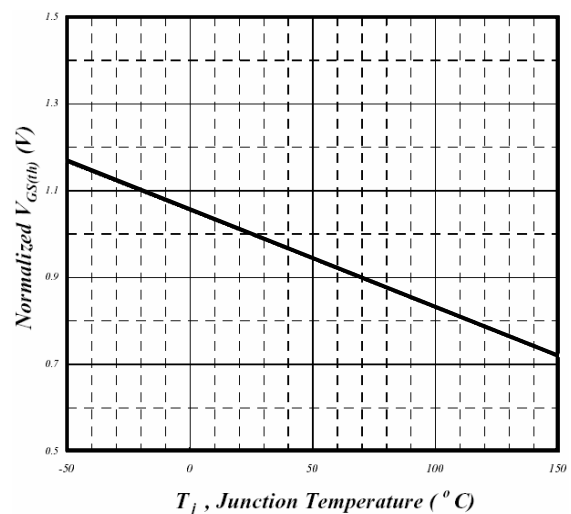


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

N-Channel

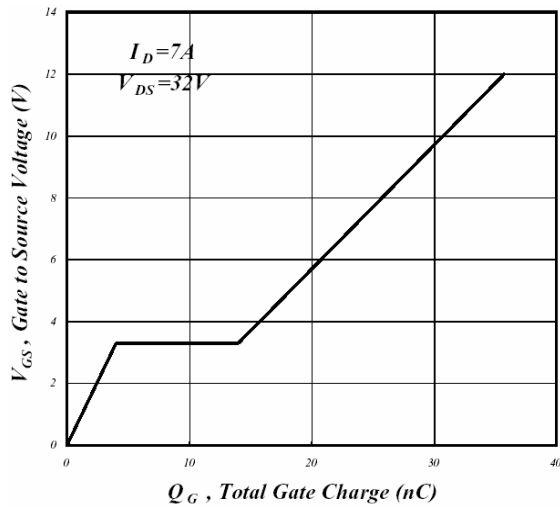


Fig 7. Gate Charge Characteristics

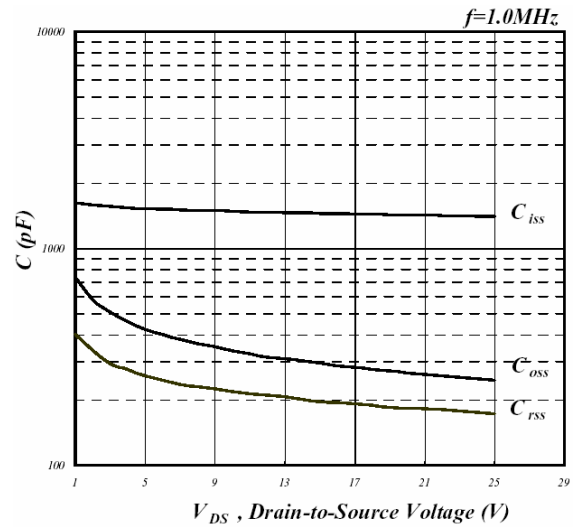


Fig 8. Typical Capacitance Characteristics

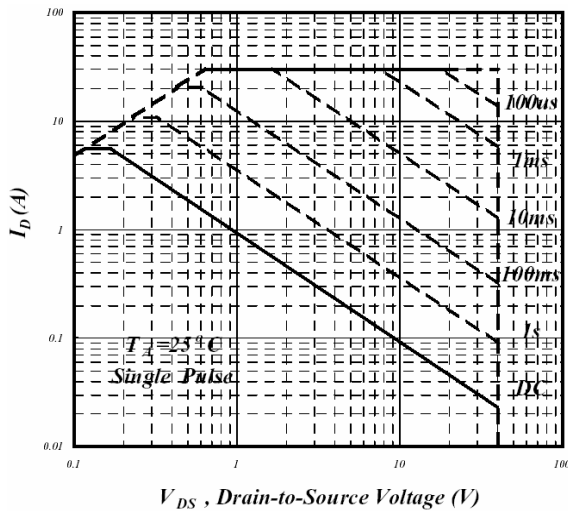


Fig 9. Maximum Safe Operating Area

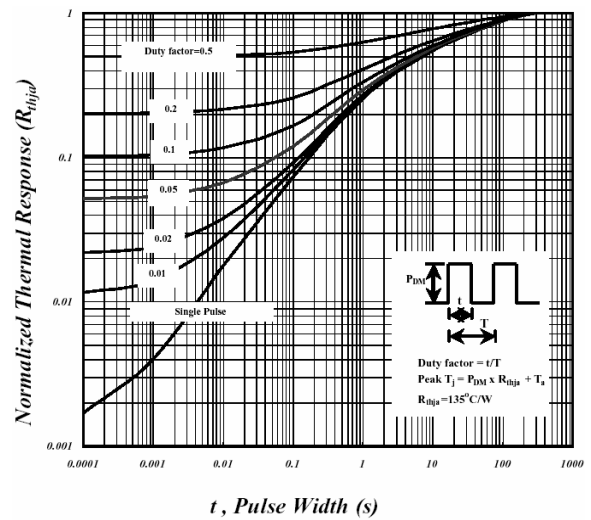


Fig 10. Effective Transient Thermal Impedance

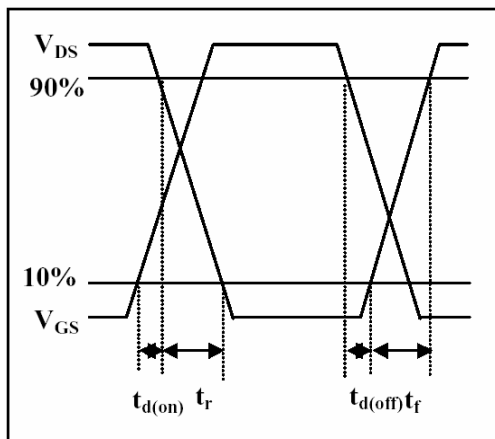


Fig 11. Switching Time Waveform

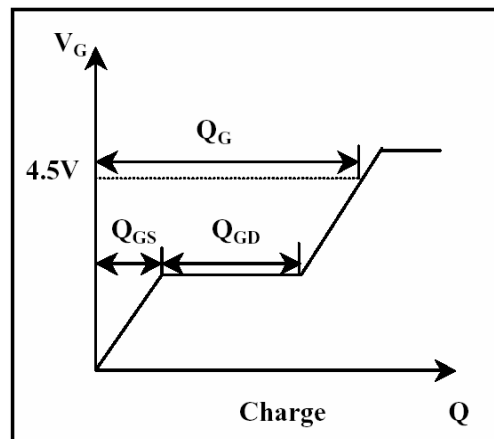


Fig 12. Gate Charge Waveform

P-Channel

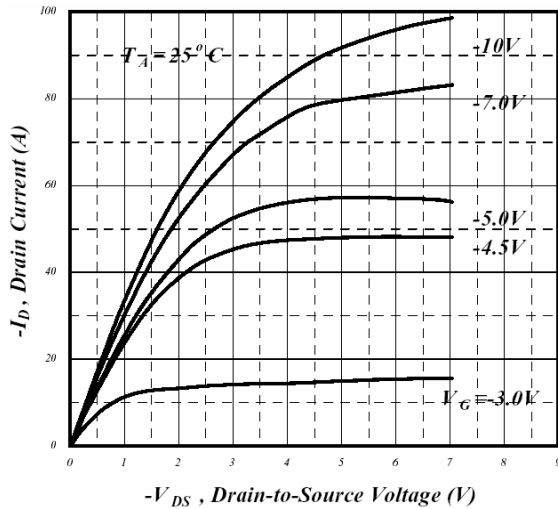


Fig 1. Typical Output Characteristics

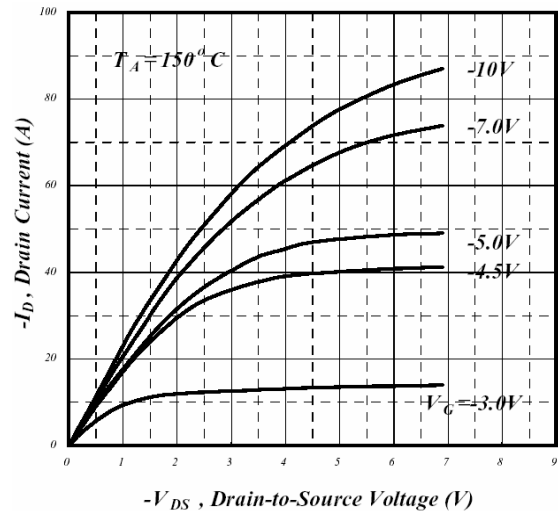


Fig 2. Typical Output Characteristics

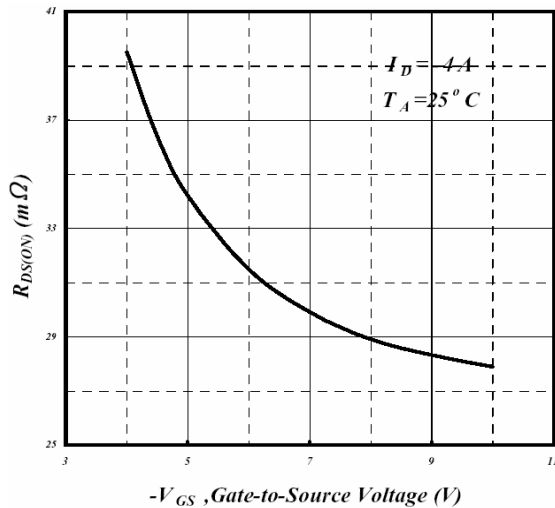


Fig 3. On-Resistance v.s. Gate Voltage

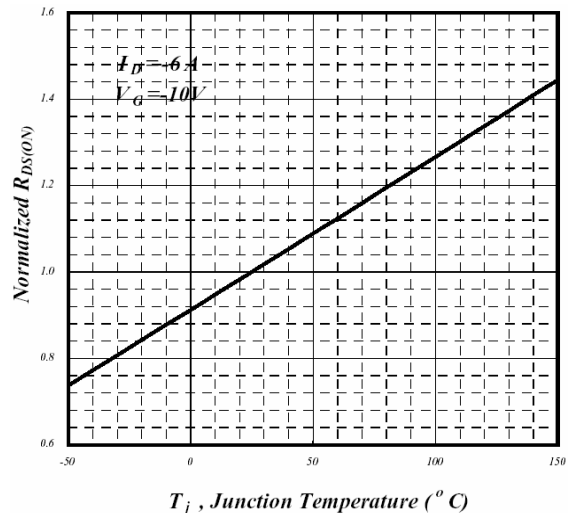


Fig 4. Normalized On-Resistance v.s. Junction Temperature

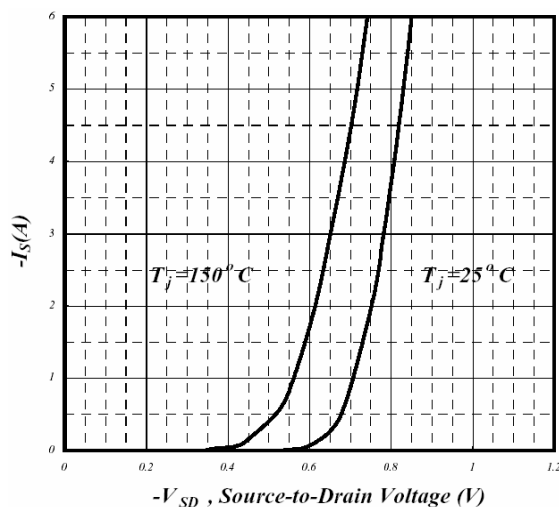


Fig 5. Forward Characteristics of Reverse Diode

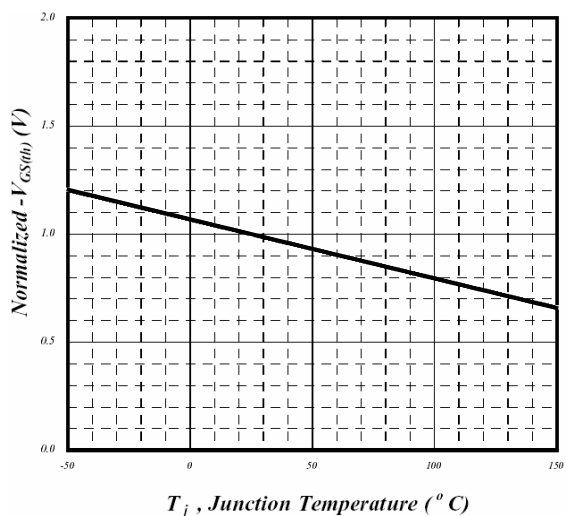


Fig 6. Gate Threshold Voltage v.s. Junction Temperature

P-Channel

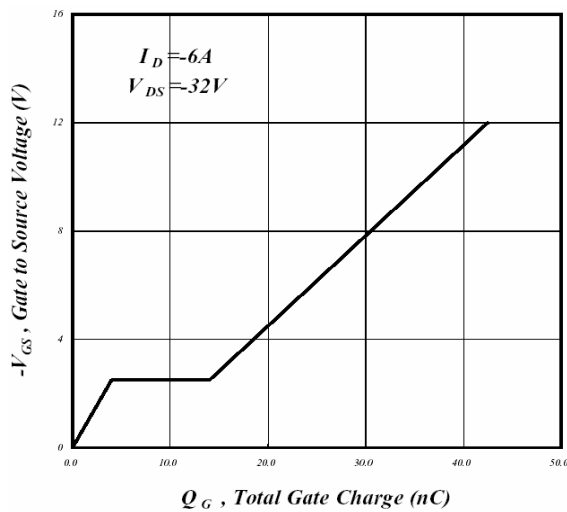


Fig 7. Gate Charge Characteristics

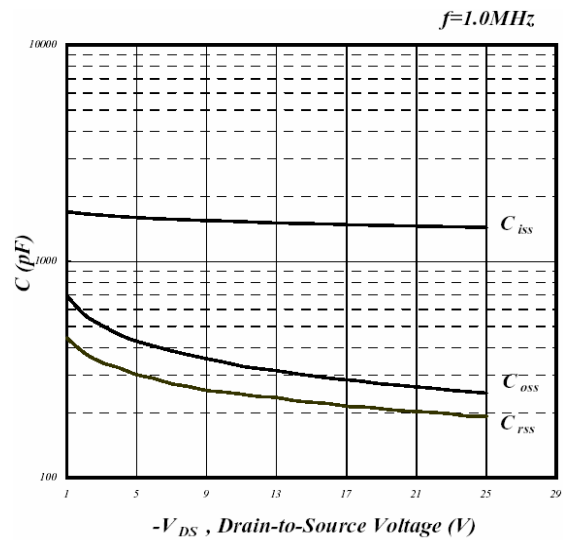


Fig 8. Typical Capacitance Characteristics

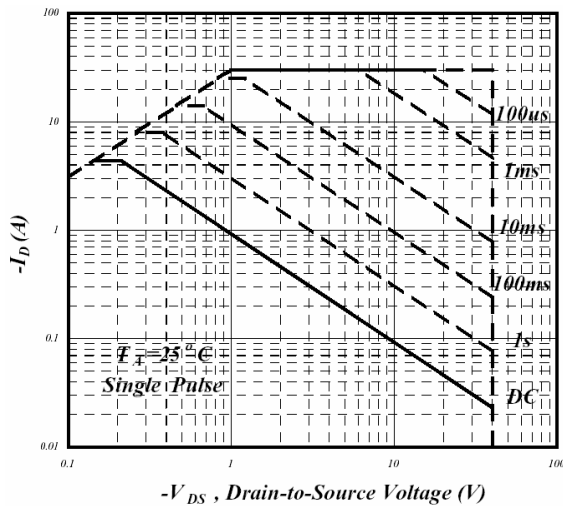


Fig 9. Maximum Safe Operating Area

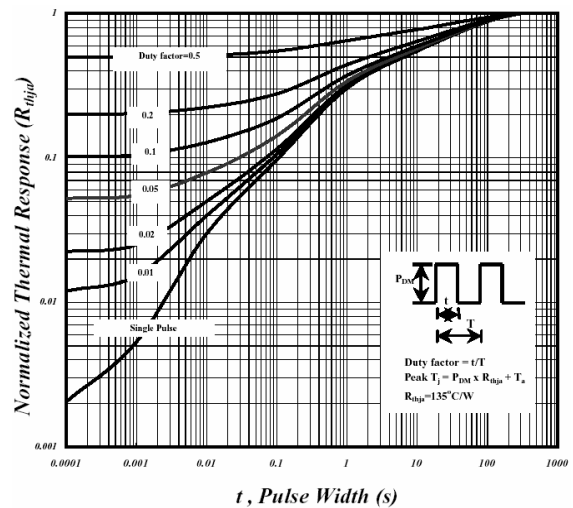


Fig 10. Effective Transient Thermal Impedance

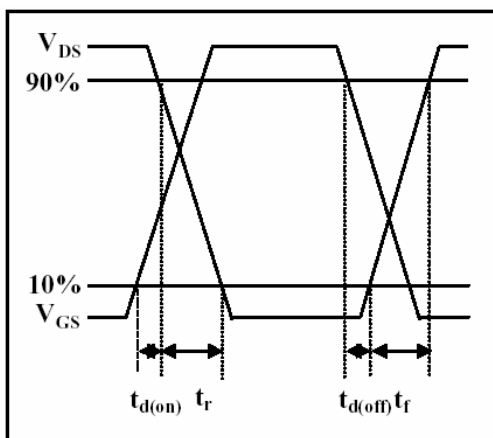


Fig 11. Switching Time Waveform

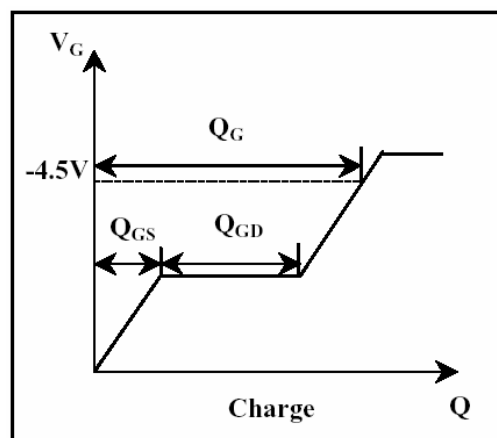


Fig 12. Gate Charge Waveform

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